WJEC Computer Science 2017 Specification Scheme of Work

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| **Week** | **Topic** | **Teaching Activity** | **Notes** |
|  | **1. Hardware**  Describe the characteristics of CPU architecture, including Von Neumann architectures.  Identify and explain the role of the components of the CPU in the fetch-decode-execute cycle.  Explain how performance is affected by the cache size, clock speed and number of cores.  Explain the difference between RISC and CISC types of processors. | Draw a Von Neumann architecture  Using a labelled CPU diagram, explain the fetch-decode-execute cycle.  Define cache, clock speed and cores. bit.ly/ahcs2kcr1P0  Use RISC Simulator bit.ly/ahcs2ku84rI | Ensure correct symbols are used to represent elements as shown in Appendix C of the specification.  Instruction set here for the development of tasks bit.ly/ahcs2kPMz5R |
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